Indian Institute of Information Technology, Allahabad

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

Course Name: Electrical Engineering Lab

EXPERIMENT NO: 1

Objective:

a) To verify the Kirchoff's voltage law and Kirchoff's current law.

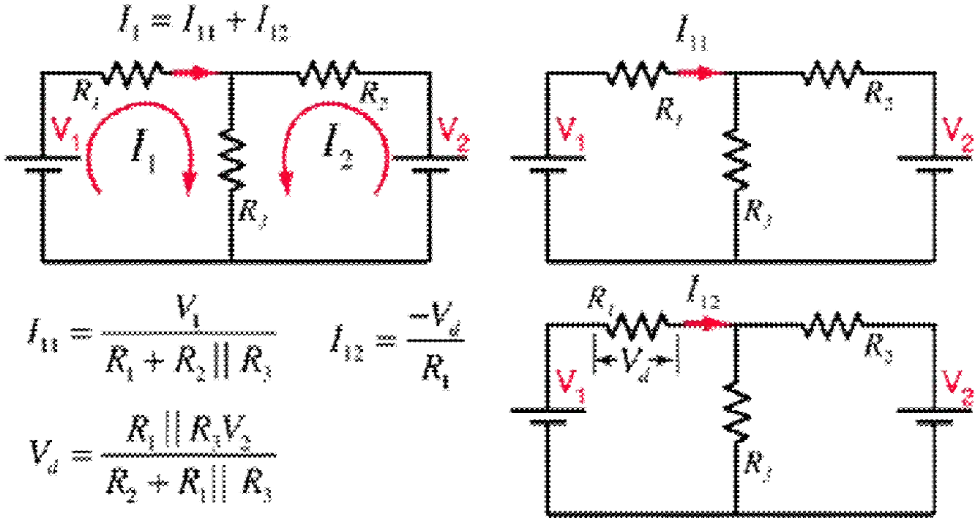
Materials/ Component Required :

Bread board, resistors, multimeter, DC power supply, connecting wires.

Theory:

KCL: KCL states that the total current entering a circuit's junction is exactly equal to the total current leaving the same junction. This idea by Kirchhoff is commonly known as the Conservation of Charge.

KVL: KVL states that for a closed loop series path the algebraic sum of all the voltages around any closed loop in a circuit is equal to zero. This is because a circuit loop is a closed conducting path so no energy is lost.



$$I_{11} = \frac{V_1}{R_1 + R_2 \| R_3} \qquad I_{12} = \frac{-V_d}{R_1}$$

$$V_d = \frac{R_3 \| R_1 V_2}{R_2 + R_1 \| R_3}$$

$R_1 \| R_3$ means the parallel resistance of R_1 and R_3.

Consider R1 = 10 k, R2 = 3.3 k and R3 = 2.7 k

And V1 = 12 V, V2 = 5 V.

Calculation:

Result: